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(54) **INTEGRATED CIRCUIT WITH MODULAR
 DYNAMIC POWER OPTIMIZATION
 ARCHITECTURE**

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 (57) **ABSTRACT**

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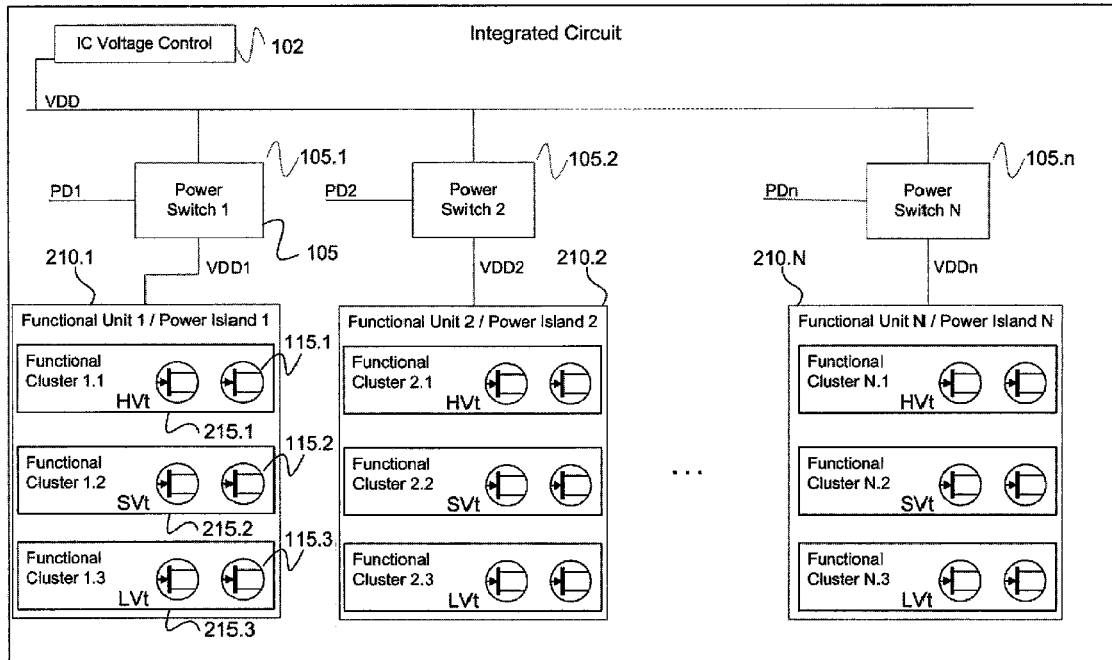
A system and method for regulating power consumption within an integrated circuit (IC) with a modular design. The IC is designed so that any one distinct functional module within the IC utilizes only transistors with a substantially same or similar critical voltage level, which may for example be the threshold voltage of the transistors. Consequently, the supply voltage delivered to each functional modules can be lowered to the minimum voltage necessary to enable the transistors within the module to operate. Similarly, modules within the IC may be designed with transistors which share a common value for a substrate bias voltage or a clock speed, or with a combination of common values for several electrical factors. In this way, it is possible to reduce power consumption by fine-tuning the voltages supplied to (or clock speeds driving) specific modules, in a way which is custom-tuned to each module.

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[0096] However, in IC 200, an exemplary functional unit 210 is now further sub-divided into two or more exemplary functional clusters 215. Each functional clusters 215 is distinguished by the fact that all transistors within the functional cluster belong to the same electrical property class. For example, the first functional cluster 215.1 is composed exclusively of transistors 115.1 which all have a high threshold voltage (HVt). The second functional cluster, 215.2 is comprised of transistors 115.2 which all have a standard threshold voltage (SVt). The third functional unit, 215.3 is comprised of transistors 115.3 which all have a low threshold voltage (LVt). As a result, each functional cluster 215 is comprised exclusively of a single type or single class of transistor having a common electrical characteristic such as those having a high threshold voltage, a standard threshold voltage, or a low threshold voltage.

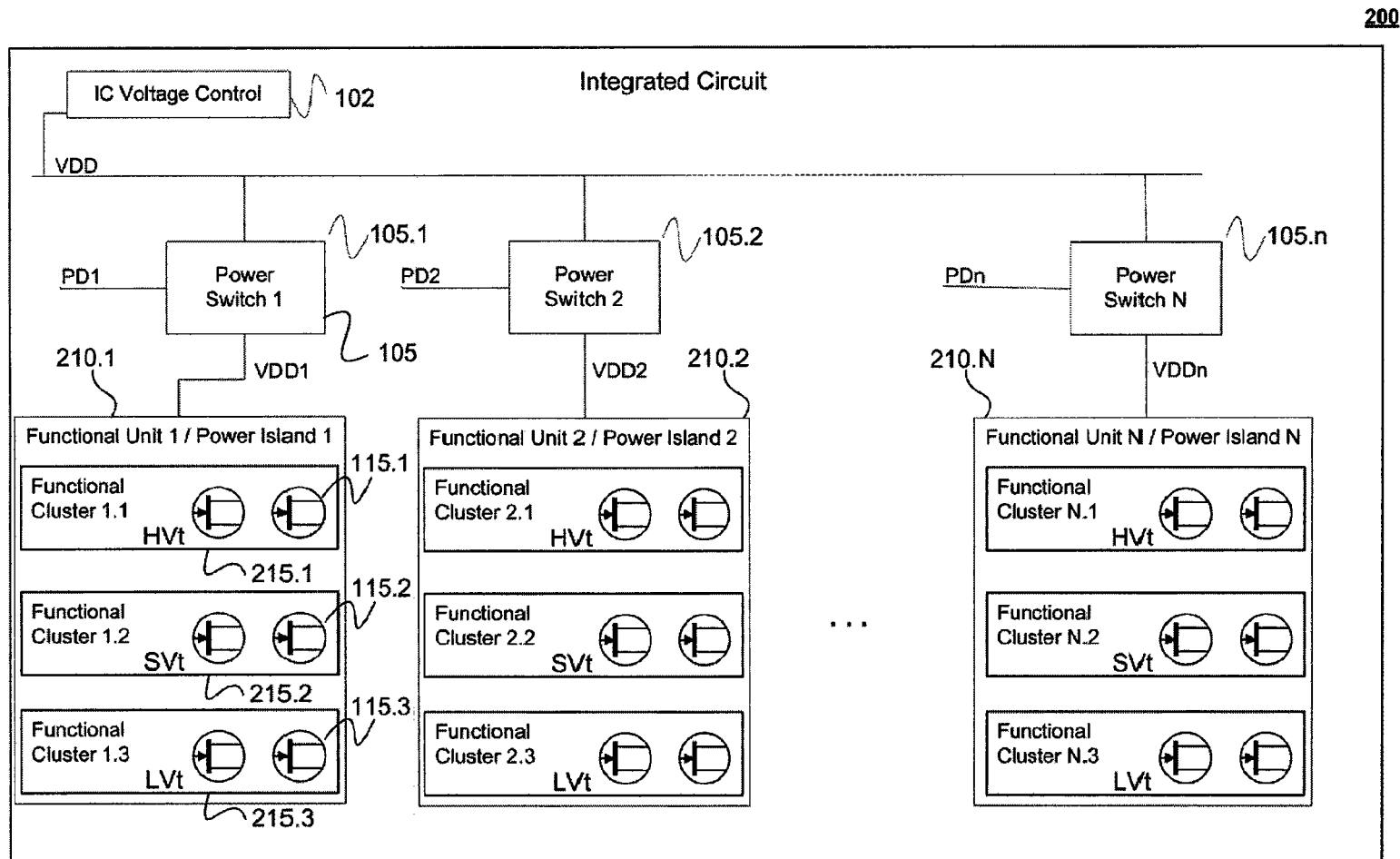


FIG. 2

[0099] In order to design a functional unit with discrete functional clusters 215, it is necessary during the design process to consider which types of functions within the functional unit 210 may lend themselves to transistors 115 of a specific electrical property class. For example, some applications may require transistors which have a high threshold voltage, while other specific applications or functions lend themselves to transistors which may require a standard threshold voltage or a low threshold voltage. (A threshold voltage is one example of a critical voltage level.)

[0113] Exemplary IC 600 includes an IC power control element 605. IC power control element 605 in turn may be comprised of a number of modules which can regulate the power consumed by each functional unit 210 and each functional cluster 215 of exemplary IC 600. Control by IC power control element 605 is exerted through general control lines GCL. An exemplary single common bus GCL is shown conveying signals from module/cluster power supply voltage control 635, module/cluster clock signal control 640, and module/cluster substrate bias voltage control 645 (all discussed further below) to functional units 215.

600

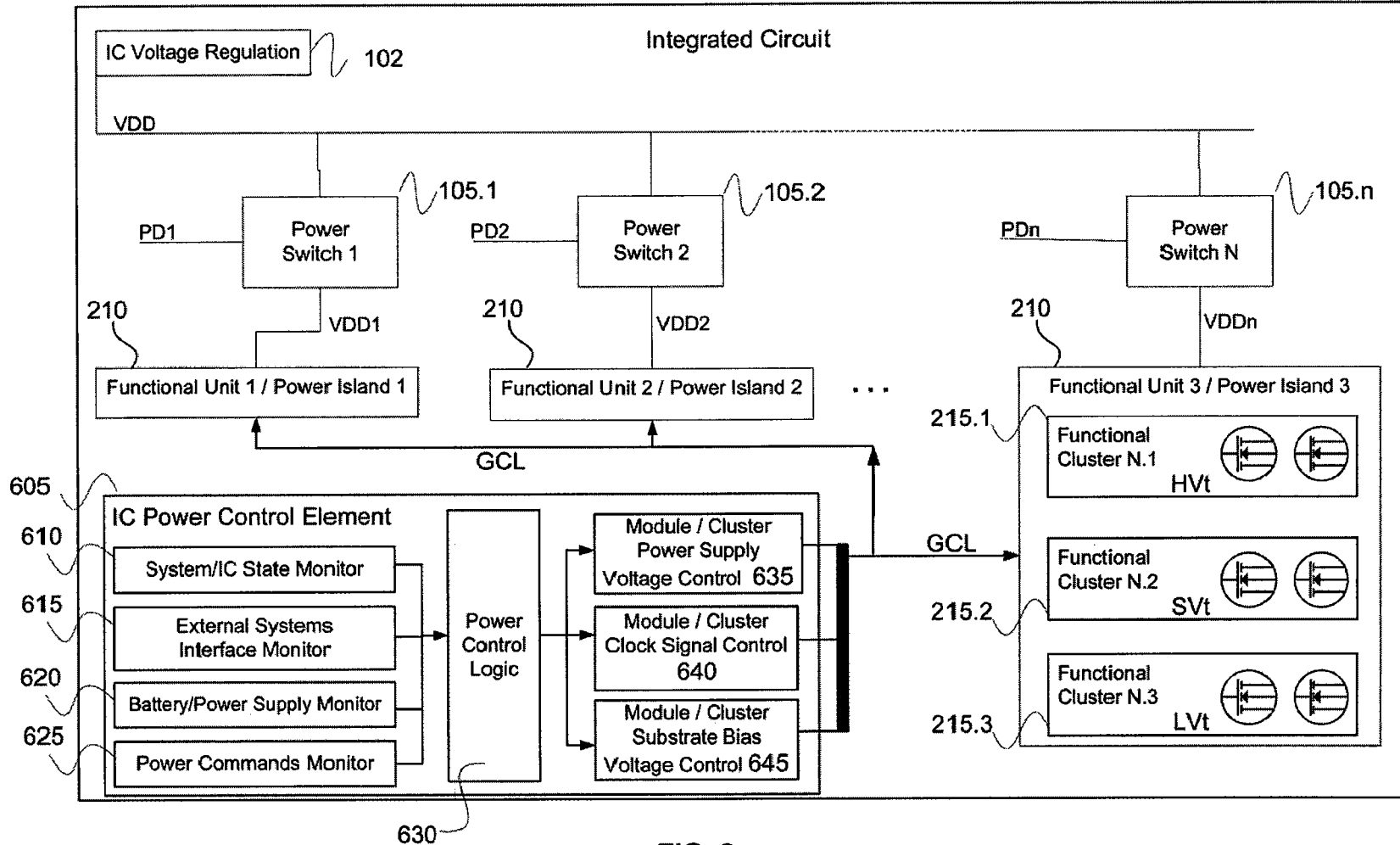


FIG. 6

[0115] System or IC state monitor 610 may serve to maintain monitor and gather status information for functions throughout IC 600. For example, IC state monitor 610 may obtain information on which functional units are currently in use, or which functional clusters are currently in use, or both or which functional clusters are likely to require a higher clock frequency within a predetermined period in order to support an application. It may also maintain information on a voltage currently being applied to functional units 210, or functional cluster 215, or similarly, on clock speeds or substrate bias voltages for functional units 210 and functional clusters 215.

[0140] FIG. 9 is a flowchart of an exemplary method 900 for designing an integrated circuit (IC) according to the present system and method. The method begins at step 905 and continues immediately with step 910. In step 910, a determination is made as to the functional requirements of the IC (also known as "applications") such that a further determination can be made as to functional units of the IC. In this way a list of functional units of the IC is created.

[0141] In step 915, a first functional unit is selected for evaluation.

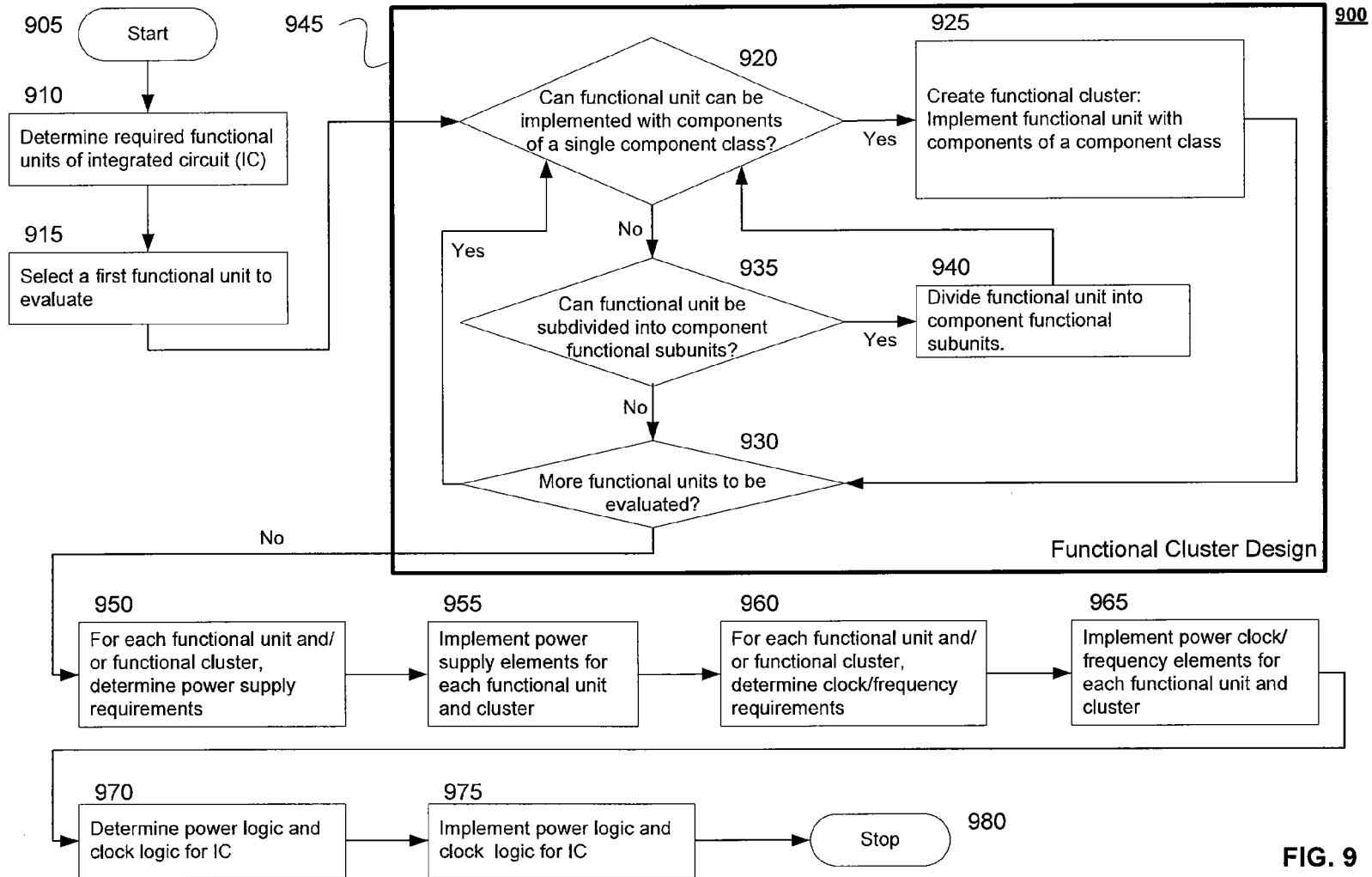


FIG. 9

INTEGRATED CIRCUIT WITH MODULAR DYNAMIC POWER OPTIMIZATION ARCHITECTURE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention pertains to the field of power management in a semiconductor environment. More particularly, the invention pertains to a system and method for adaptive scaling of voltages, clock speeds, and other electrical factors within an integrated circuit in order to dynamically minimize power consumption while maintaining optimum performance.

[0003] 2. Background Art

[0004] For virtually all electronics applications, it is desirable to minimize power consumption. In terms of system design and performance, reduced power consumption results in less heat being generated. This increases system life, reduces requirements for cooling systems. A reduction in power supply requirements also enables smaller, more compact design. Further, any reduction in the power consumed by a circuit component, such as an integrated circuit (IC) or a module within an IC, will improve the performance and reliability of prior circuit stages which feed into the IC or IC module. Further, for portable devices such as laptop computers, media players, and cell phones, reduced power consumption contributes to longer battery life and also enables additional functionality for a given power supply. From a societal standpoint, even incremental reductions in power consumption contribute to conservation of energy resources.

[0005] There are a number of conventional strategies for reducing power consumption within integrated circuits. One strategy is to identify a module(s) within an IC which has not drawn power for some determined period of time, or which is not anticipated to draw power for some future period of time (or both), and to either reduce or shut off the power supply to the module. If the module is fed by a single power supply, then this strategy may only be viable if no components or submodules within the module are expected to require power during this period of time. If any submodule or component within the module is expected to require power, it may be necessary to maintain a supply of power to the entire module. (In some cases, the "module" may constitute the entire IC as a whole.)

[0006] Another conventional power reduction strategy is to reduce the power supplied to the IC or to a module within the IC. In virtually all cases, this will result in some kind of reduction in system performance, for example lower clock speeds for digital chips or reduced range for a radio frequency (RF) chip. Depending on the application for which the IC is being used, or depending on the particular function of a module within an IC, in some cases the reduction in system performance will have no noticeable impact from a user perspective. For example, a user using a portable computer for word processing may not notice a reduction in the clock speed of the system microprocessor. Clearly, however, for some applications—such as popular video applications or voice-to-text translation, to name just two of many examples—it is desirable to maintain maximum performance from an IC, for example, to maintain maximum clock speed from a microprocessor or a Digital Signal Processor (DSP) chip. For these applications, any attempts at power savings through reduced supply voltages may have a notable impact, and sometimes an unacceptable impact, on system performance in relation to the requirements of the user application.

[0007] What is needed, then, is a system and method for providing on-chip power management for an integrated circuit, where the system and method minimize any negative impact on system performance, and where the system and method take better advantage of the variable levels of voltages or clock speeds which may be required by transistors and other elements within the IC package.

BRIEF SUMMARY OF THE INVENTION

[0008] The present invention meets the above-identified needs by providing a system and method for regulating power consumption within an integrated circuit (IC). In one exemplary embodiment, CMOS transistors are employed, where the CMOS transistors have two or more different threshold voltages, for example, a first threshold voltage and a second threshold voltage. The IC is designed so that any one or more distinct functional modules within the IC utilize only CMOS transistors with a single threshold voltage (for example, only a low threshold voltage or only a high threshold voltage). Consequently, the supply voltage delivered to the distinct functional modules can be lowered to the minimum voltage necessary to enable the transistors within those module to operate.

[0009] Similarly, modules within the IC may be designed with transistors which share a common source for a substrate bias voltage or a clock speed, or with a combination of common values for several electrical factors (supply voltage, substrate bias voltage, clock speed, etc.). In this way, it is possible to reduce power consumption by fine-tuning the voltages supplied to (or clock speeds driving) specific modules in a way which is custom-tuned to each module.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

[0010] The features and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference numbers indicate identical or functionally similar elements. The left-most digit of a reference number identifies the drawing in which the reference number first appears (for example, an element labeled **310** typically first appears in the drawing labeled FIG. 3).

[0011] Additionally, some elements are identified by a number followed by a period, which is then followed by a second number (for example, **215.1**, **215.2**, **215.3**, . . . , **215.n**). In these cases, the number to the left of the period (for example, "215") identifies a generic class or generic version of an element, while the number to the right of the period (for example, "1", "2", "3", . . . , "n") may identify a specific instance of the element, where the specific instance may have a further distinguishing feature or characteristic in addition to the generic qualities.

[0012] FIG. 1 is a block diagram of an exemplary integrated circuit (IC).

[0013] FIG. 2 is a block diagram of an exemplary IC according to the present system and method.

[0014] FIG. 3 is a block diagram of an exemplary functional cluster within an IC according to the present system and method.

[0015] FIG. 4 is a block diagram of an exemplary functional cluster within an IC according to the present system and method.

[0016] FIG. 5 is a block diagram of an exemplary functional cluster within an IC according to the present system and method.

[0017] FIG. 6 is a block diagram of an exemplary IC according to the present system and method.

[0018] FIG. 7 is a block diagram of an exemplary IC according to the present system and method.

[0019] FIG. 8 is a block diagram of an exemplary IC according to the present system and method.

[0020] FIG. 9 is a flowchart of an exemplary method for designing an IC according to the present system and method.

[0021] FIG. 10 is a flowchart of an exemplary method for allocating power on an IC according to the present system and method.

DETAILED DESCRIPTION OF THE INVENTION

- [0022]** 1. Introduction
- [0023]** 2. Definitions
- [0024]** 3. Exemplary Integrated Circuit (Conventional)
- [0025]** 4. Overview of the Present System and Method
- [0026]** 5. Exemplary Integrated Circuit (IC) According to the Present System and Method
- [0027]** 6. Another Exemplary IC
- [0028]** 7. Another Exemplary IC
- [0029]** 8. Another Exemplary IC
- [0030]** 9. An Exemplary Method for Designing an IC
- [0031]** 10. Exemplary Method for Real Time Dynamic Power Minimization for an IC
- [0032]** 11. Alternative Embodiments
- [0033]** 12. Conclusion

1. Introduction

[0034] The present invention is directed to systems and methods for using a modular organization of electrical components within an integrated circuit (IC) to minimize IC power consumption while maintaining substantially optimal performance by the IC.

[0035] Some systems or methods may be defined or characterized here in whole or in part by exemplary instances of such systems or methods (for example, by an IC with a particular organization of modules and submodules, or a particular organization or type of electrical components such as transistors, or by a method with a particular set of steps). It should be understood, however, that such systems or methods may encompass other specific instances or embodiments not specifically described herein.

2. Definitions

[0036] Functional unit—An integrated circuit (IC) may perform just a single function, for example by serving as a flip-flop or an adder. Typically, however, an IC employing large scale integration (LSI) or very large scale integrated (VLSI) may perform multiple functions on a single chip. A module comprising a group of components (for example, transistors, resistors, capacitors, diodes, and/or inductors) on an IC which perform a defined function may be regarded as a “functional unit”. A functional unit may typically, though not necessarily, have a specific set of inputs and outputs, and a well-defined interface (an electrical interface, a logical interface, and/or other interfaces) with other functional units of the IC, or with external components, or both.

[0037] There may be repeated instances of a single function (for example, multiple flip-flops or adders on a single chip), or

there may be two or more different types of functional units which together provide the IC with its overall functionality. For example, a microprocessor may have such functional units as an arithmetic/logic unit(s) (ALU), a floating point unit(s) (FPU), a load/store unit(s), a branch prediction unit(s), a memory controller(s), and other such modules. Each of these modules within the IC may be regarded as a distinct functional unit, and some such units may be further subdivided into component functional units. At a higher level, a microprocessor as a whole may be viewed as a functional unit of an IC, for example if the microprocessor shares the IC die with at least one other functional unit, for example, a cache memory unit.

[0038] Some other possible functional units may include, for example and without limitation, a general purpose processor, a mathematical processor, a state machine, a digital signal processor, a video processor, an audio processor, a logic unit, a logic element, a multiplexer, a demultiplexer, a switching unit, a switching element, an input/output (I/O) element, a peripheral controller, a bus, a bus control, a register, a combinatorial logic element, a storage unit, a programmable logic device, a memory unit, a neural network, a sensing circuit, a control circuit, a digital to analog converter, an analog to digital converter, an oscillator, a memory, a filter, an amplifier, a mixer, a modulator, or a demodulator.

[0039] Persons skilled in the relevant arts will recognize that there are many other well-known types of functional units which may be employed as part of electronic modules implemented in an IC, and the list provided above is only a representative sampling of such functional units. Any such functional units, and possibly others yet to be developed, may conceivably serve as elements of the present system and method, and benefit from the power management techniques of the present system and method, as described below.

[0040] A functional unit may occupy a specific, localized area of an IC die, with a well defined geometric boundary on the die. However, a functional unit may also be distributed over the die, with two or more localized, coupled sets of components which together provide the functionality of the functional unit.

[0041] Functional cluster—A functional cluster as defined in this document is similar to a functional unit.

[0042] Specifically, a “functional cluster” is a module or group of components (for example, transistors, resistors, capacitors, diodes, and/or inductors) on an IC which perform a defined function. Those functions may possibly include but are not limited to those functions enumerated immediately above in conjunction with the definition of “functional unit”. However, a “functional cluster” is specifically further defined by including some class of components (for example, a class of transistors) that have at least one similar electrical characteristic and behave similarly in response to such electrical factors as supply voltage, current, clock speed, or substrate bias voltage.

[0043] For example, in a functional cluster, all the transistors may have a same or substantially similar threshold voltage. Or, for another example, in a functional cluster, all the transistors may have a same or substantially similar input impedance, or a same or substantially similar maximum clock speed or minimum clock speed corresponding to supply voltages. The elements which have the same or substantially the same electrical response to an electrical input factor may be referred to as an “electrical property class”. This term is discussed further below.

clusters) may have a same functionality, a similar functionality, or a different functionality of a second functional cluster of the two or more functional clusters. In some embodiments of the present system and method, two or more functional clusters may be specifically configured to provide a same function or substantially similar functionality, but with different performance parameters and with correspondingly different power requirements.

[0180] For example, a microprocessor may be configured with a first memory system (such as a cache memory) and a second memory system (such as a second level cache), but with the first cache memory configured for a higher speed of data storage and data retrieval than the second level cache memory. The higher speed memory will, typically, require higher power. The microprocessor may determine when a current application requires higher speed memory access, and employ the higher speed cache for that purpose. The microprocessor may also determine when a current application may meet its performance requirements with lower speed data access, and so may switch memory operations to the lower speed, lower power cache. A similar example may be a microprocessor configured with two (or more) redundant arithmetic units, the first configured for higher speed, higher power calculations, and the second configured for lower speed, lower power calculations. The appropriate arithmetic unit (higher speed or lower speed) may be called into play as application requirements demand or permit, respectively.

12. Conclusion

[0181] As will be appreciated by persons skilled in the relevant art(s), the system(s) and method(s) described here represent only one possible embodiment of the present invention. Many of the elements described herein could, in alternative embodiments of the present invention, be configured differently within the scope and spirit of the present invention. In addition, additional elements, or a different organization of the various elements, could still implement the overall effect and intent of the present system and method. Therefore, the scope of the present invention is not limited by the above disclosure and detailed embodiments described therein, but rather is determined by the scope of the appended claims.

What is claimed is:

1. An integrated circuit (IC) comprising:
 - a plurality of functional clusters, wherein each functional cluster has a respective critical voltage level; and
 - one or more voltage supply elements configured to supply each functional cluster with a respective regulated voltage;
 - wherein each respective regulated voltage determines a respective operational state of a corresponding functional cluster of the plurality of functional clusters based on a level of the respective regulated voltage in relation to the respective critical voltage level of the functional cluster.
2. The IC of claim 1, wherein the functional cluster comprises a plurality of electrical components that substantially share the respective critical voltage level of the functional cluster.
3. The IC of claim 2, wherein the plurality of electrical components comprises a plurality of transistors.
4. The IC of claim 3, wherein the respective critical voltage level is a respective threshold voltage of the transistors.

5. The IC of claim 4, wherein:

- a respective regulated voltage equal to or above the respective supply threshold voltage of the transistors is delivered to the transistors to set an on-state of the functional cluster; and

- wherein a respective regulated voltage less than the respective supply threshold voltage of the transistors is delivered to the transistors to set an off-state of the functional cluster.

6. The IC of claim 3, wherein the respective critical voltage level is a respective substrate bias voltage of the plurality of transistors.

7. The IC of claim 6, wherein a power consumption of the respective functional cluster is minimized by setting the respective substrate bias voltage to a value which minimizes a leakage current of the respective functional cluster.

8. The IC of claim 1, wherein at least a first respective critical voltage level of a first functional cluster is different from a second respective critical voltage level of a second functional cluster.

9. The IC of claim 1 wherein the respective operational state is at least one of an on-state, an on state with a reduced power consumption, an on-state with a minimal power consumption, an off-state, or a frequency of operation of the respective functional cluster.

10. The IC of claim 9, wherein the on-state is determined by at least one of:

- the respective regulated voltage being equal to the respective critical voltage level; or

- the respective regulated voltage being greater than the respective critical voltage level.

11. The IC of claim 1, wherein the respective critical voltage level is a minimum voltage level consistent with maintaining a selected operational frequency of the respective functional cluster.

12. The IC of claim 11, wherein the respective functional cluster is configured so that increasing the respective regulated voltage increases a maximum obtainable frequency of operation of the respective functional cluster.

13. The IC of claim 1, further comprising one or more frequency control elements, wherein one or more functional clusters of the plurality of functional clusters have one or more respective frequency control elements.

14. The IC of claim 13, wherein the IC is configured to reduced power consumption by the one or more functional clusters by using the respective one or more frequency control elements to reduce a respective frequency of operation of the one or more functional clusters.

15. The IC of claim 1, further comprising a control element configured to minimize a power consumption of the IC by at least one of:

- determining the regulated voltage supplied to the functional cluster; or

- determining the substrate bias voltage to the functional cluster; or

- determining a frequency of operation of the functional cluster.

16. The IC of claim 15, wherein the control element comprises control logic configured to dynamically minimize the power consumption of the IC in response to at least one of an operational requirement of the IC, an operational condition of the IC, or an operational environment of the IC.

17. The IC of claim 1, wherein a functional cluster comprises at least one of a general purpose processor, a microprocessor, a mathematical processor, an arithmetic/logic unit,

a state machine, a digital signal processor, a video processor, an audio processor, a logic unit, a logic element, a multiplexer, a demultiplexer, a switching unit, a switching element, an input/output (I/O) element, a peripheral controller, a bus, a bus control, a register, a combinatorial logic element, a programmable logic device, a memory unit, a neural network, a sensing circuit, a control circuit, a digital to analog converter, a gate, a plurality of gates, an analog to digital converter, an oscillator, a memory, a filter, an amplifier, a mixer, a modulator, or a demodulator.

18. The IC of claim **1** wherein the plurality of functional clusters comprises a first functional cluster and a second functional cluster, and wherein:

the second functional cluster is configured to provide a functionality which is at least partially redundant with a functionality of the first functional cluster, and

the second functional cluster is configured to provide the redundant functionality at a lower power consumption than the first functional cluster.

19. The IC of claim **1**, wherein a voltage supply element of the one or more voltage supply elements comprises an on-chip power supply.

20. The IC of claim **19**, wherein at least two functional clusters of the plurality of functional clusters are configured to share a common on-chip power supply.

21. The IC of claim **1**, wherein a voltage supply element of the one or more voltage supply elements comprises a bus for delivering voltage from an off-chip power supply.

22. The IC of claim **1**, further comprising a plurality of voltage supply elements, wherein at least two functional clusters of the plurality of functional clusters are supplied with respective regulated voltages from different respective voltage supply elements.

23. A method for designing an integrated circuit (IC) for reduced power consumption, comprising:

determining a required functional cluster of the IC;

determining that the functional cluster can be implemented with a plurality of electrical components sharing a substantially same critical voltage level; and

implementing the functional cluster with the plurality of electrical components sharing the substantially same critical voltage level.

24. The method of claim **23**, further comprising:

for a functional cluster which cannot be implemented with a plurality of electrical components sharing a substantially same critical voltage level, evaluating whether the functional cluster can be subdivided into a plurality of functional subunits, wherein at least one of the functional subunits can be implemented with a second plurality of electrical components sharing a second substantially same critical voltage level.

25. The method of claim **24**, further comprising:

implementing the functional subunit as a functional cluster with the second plurality of electrical components sharing the second substantially same critical voltage level.

26. The method of claim **23**, further comprising:

for each functional cluster of the IC repeating the step of determining that the functional cluster can be implemented with a plurality of electrical components sharing a substantially same critical voltage level; and repeating the implementation step for each functional cluster which can be implemented with the plurality of electrical components sharing the substantially same critical voltage level.

27. The method of claim **23**, further comprising implementing a voltage supply for the functional cluster which can be implemented with the plurality of electrical components sharing the substantially same critical voltage level, wherein the voltage supply is configured to deliver a minimum voltage necessary to meet the critical voltage level of the functional cluster.

28. The method of claim **23**, further comprising implementing a clock for the functional cluster which can be implemented with the plurality of electrical components sharing the substantially same critical voltage level, wherein the clock is configured to deliver a frequency which minimizes a power requirement of the functional cluster.

29. In an integrated circuit (IC) configured with a plurality of functional clusters, wherein each functional cluster comprises a plurality of electrical components sharing a substantially same critical voltage level, a method for minimizing power consumption of the IC, comprising:

determining a real-time functional requirement of the IC;

determining a functional cluster required to support the real-time functional requirement;

delivering to the functional cluster a minimum voltage which may be delivered to the functional cluster to meet a critical voltage requirement of the functional cluster.

30. The method of claim **29**, further comprising determining a minimum clock frequency which may be delivered to the functional cluster to support the real-time functional requirement.

31. The method of claim **29**, further comprising turning off a power to a functional cluster which is not required to meet the real-time functional requirement.

32. The method of claim **29**, further comprising adjusting a substrate bias voltage of a plurality of transistors of the functional cluster to minimize a leakage current.

33. The method of claim **29**, wherein the critical voltage requirement is a threshold voltage of a plurality of transistors of the functional cluster, and the minimum voltage is a minimum supply voltage necessary to meet the threshold voltage.

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